From February 2006 *High Frequency Electronics*

High-Efficiency Linearized LDMOS Amplifiers Utilize the RFAL Architecture

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This article provides design and measured performance details for a power amplifier using a recently-developed technique for distortion cancellation

The latest base station amplifier designs for the wireless telecom industry offer much higher data rate services with lower levels of distortion than preceding designs, providing high efficiency and reliable long life at lower cost. These amplifiers are also required to be economical and work reliably over a wider range of environmental conditions than the typical air-conditioned ground-based stations. Efficiency and thermal issues are critical to the type of power amplifier selected for these newer applications.

There are many amplifier types and architectures used for amplifying complex modulated signals. Each type has different levels of efficiency, acceptable distortion, complexity and cost:

- Linear Class A Amplifiers
- Linear Class AB Amplifiers
- Parallel or Serial Combined Amplifiers
- Doherty Amplifiers
- Cartesian Loop
- EE&R (Envelope Elimination & Restoration)
- LINC/CALLUM (Linear Amplification using Non-Linear Components) / (Combined Analog Locked-Loop Universal Modulator)
- Cross-Cancellation Amplifiers
- HAT (High Accuracy Tracking)
- Predistortion Amplifiers
- Feedforward Amplifiers
- RFAL Amplifiers (Reflect Forward Adaptive Linearizer)

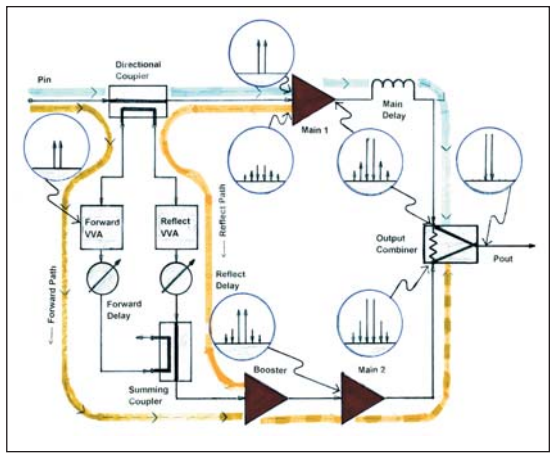

Figure 1 · Block diagram showing the RFAL architecture.

These types of amplifiers each have advantages and disadvantages when used in different applications. The pros and cons of these design techniques have been discussed in many previously published papers (see references). Frequently, many of the amplifier types listed are used within another, such as in "feedforward" and "nested-loop feedforward" amplifier configurations.

The RFAL amplifier (Reflect Forward Adaptive Linearizer) is a recently patented linearization technique that uses the information present in the reflected input signal of the first amplifier (Main 1) to create a correction signal feeding a second identical amplifier (Main 2). This significantly reduces all the distortion products of the RFAL power amplifier assembly while doubling the fundamental output power of the Main 1 amplifier. A simplified block diagram is outlined in Figure 1.

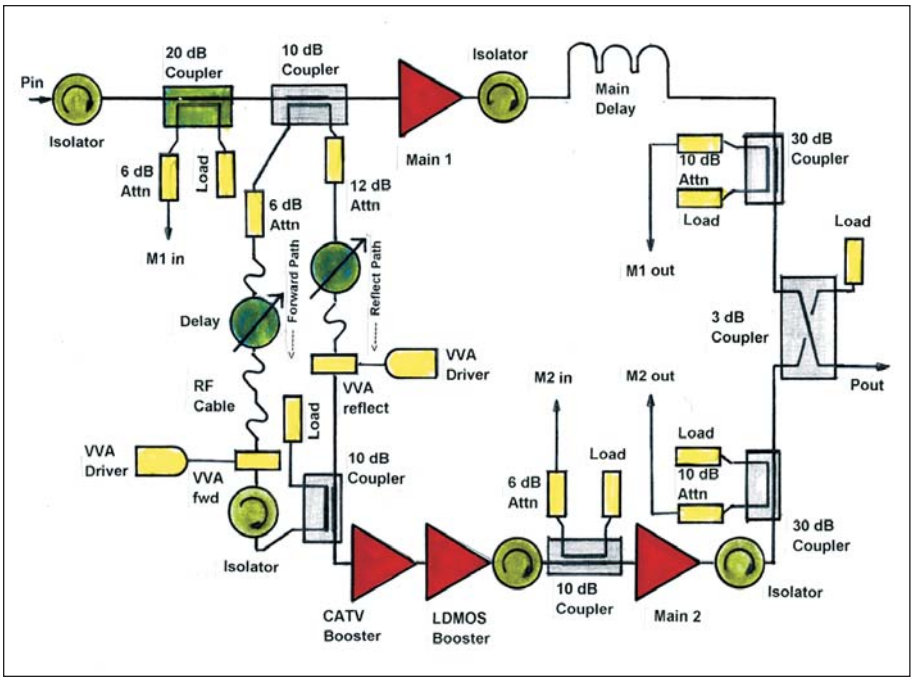

Figure 2 · Block diagram of the RFAL LDMOS amplifier assembly.

This technique was first published in the June 2004 issue of *High Frequency Electronics,* "The RFAL Technique for Cancellation of Distortion in Power Amplifiers." It was also disclosed under USA Patent #6,573,793.

The recent work described in this article uses LDMOS Class AB transistors to achieve a high level of IMD cancellation with high efficiency. The circuit configuration used is shown in the block diagram in Figure 2.

The RFAL circuit provides 18 dB of flat gain across the 865 to 895 MHz frequency range with 40 watts PEP or +43 dBm average and IMD better than 48 dBc (two tones input, each at +22 dBm average spaced at 100 kHz).

The LDMOS RFAL achieves a significant IM3 improvement of over 15 dB and a total overall efficiency of >20% above the +43 dBm average P_{out} level (Figure 3). The higher order 5th and 7th IMD term improvement were not as significant as the 3rd order IMD because the two amplifiers used, Main 1 and Main 2, are not well matched in their input non-linear characteristics. This issue is discussed in more detail later in the section titled "Further Improvements in IMD."

Over the frequency range from 865 to 895 MHz the IM3 improvement at a P_{out} of +43 dBm average is over 16 dB. Efficiency remains at around 20% over the frequency range for power levels above +43 dBm (Figure 4).

Figure 5 shows the RFAL multitone performance at composite average P_{out} of +38.5 dBm using 8 carriers signals spaced at 300 kHz (input signals from a RDL MTG-2000 multitone generator were peaked phase aligned, and the spectrum analyzer at max hold). The RFAL shows significant IMD cancellation improvement of the Main 1 and Main 2 signals while the fundamental signals are nearly doubled.

An important feature of the RFAL is that it can operate the LDMOS amplifiers well into the non-linear range of the transistors where the efficiency is high. At this power level

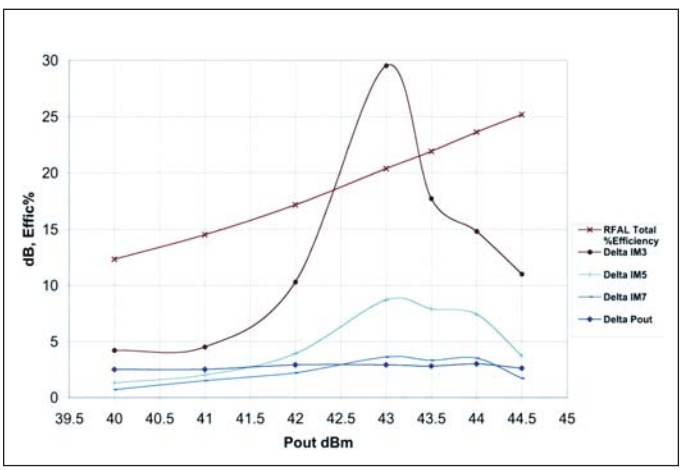

Figure 3 · IMD and P_{out} Delta improvement for RFAL vs. Main 1 amplifier and RFAL total percent efficiency. (Composite average P_{out} of two tones at f_c = 880 MHz spaced as 0.1 MHz.)

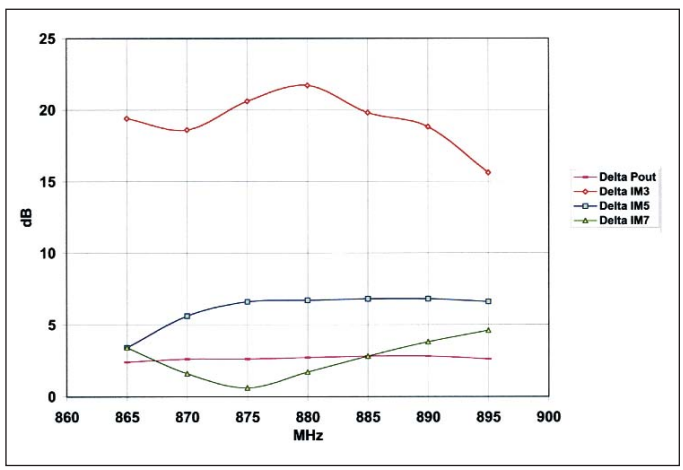

Figure 4 · IMD and P_{out} Delta improvement for RFAL vs. Main 1 amplifier. (P_{out} = 20 watts average, two tones of +40 dBm each spaced at 0.1 MHz, across the 865-895 MHz band.)

the RFAL can still provide an acceptable level of IMD cancellation. Other advantages include lower transistor power dissipation that relates to higher MTBF, two separate heat sources for simplified cooling design requirements, and use of lower power transistors to achieve the desired operating power at lower costs.

RFAL Component Description

Main Amplifiers—The single stage LDMOS Class AB amplifiers designated Main 1 and 2 as shown in the block diagram in Figure 2 use the Agere AGRA-0945-XUM plastic package transistor and is rated at 45 watts PEP at 1 dB CP. The transistors on both Main amplifiers are biased at V_d = 28V and $I_q \approx$ 400 mA. The combined Main amplifiers (excluding the Booster amplifiers) operate at approximately 28% efficiency with a P_{out} of 20 watts average composite of two tones and a 35 dBc IM3 C/I for each amplifier (without the reflect path correcting signal). When used in the RFAL configuration, the transistors can be operated up to the 2 dB back-off point with significant IMD cancellation, as shown in Figure 4.

Booster Amplifiers—Two amplifiers, consisting of a 1 GHz CATV CA901 hybrid module driving a single stage Freescale MRF282S LDMOS 10 watt PEP transistor. This lineup provides linear drive to the Main 2 amplifier up to the +26 dBm output level with better than 55 dB C/I. The Booster amplifiers operate at +28 volts at 0.95 amp total and dissipate 26.6 watts of the total 50.4 watts used by the RFAL assembly. No thermal compensation was used with this line up. A high degree of thermal compensation, AGC, or adaptive control circuitry will be required to operate the RFAL over a wide temperature range.

Couplers—Anaren Xinger microstrip PCB mounted couplers were used for the 3 dB, 10 dB, 20 dB, and 30 dB couplers.

Phase Shifters—The phase shifters were made using PCB mount Soshin Electric Co GSC362-HYB0900 3 dB quad couplers with Tronser sapphire trimmers. The coupler thru lines is connected to variable capacitors at each end, and the coupled line provides the input and output terminals. The configuration allows up to 20 degrees of phase shift with minimum attenuation change.

VVA Attenuators—The low distortion VVA consists of a four-diode π-type attenuator using Agilent HSMP-3814BLK pin diodes. (Refer to Figure 3 of Avago Technologies [formerly Agilent/HP semiconductor components group] Application Note #1048.) The VVA could be replaced with fixed attenuation values with the same electrical delay after the final alignment value is set. A temperature compensated attenuator could also be used to compensate for the gain variation of the Booster amplifier chain. The power dissipation of the VVA/Driver is low and was not included in total RFAL current.

Isolators—The Isolators were used to provide good isolation and transistor protection while aligning the circuit. It is possible to remove these isolators after the circuit works properly across the desired frequency range. The main delay and forward path delay will have to be adjusted to achieve the same electrical delay as before. The circuit uses Alcatel Ferrocom Model 9A72-31 (850 to 950 MHz) circulators with 50-ohm loads.

Delay Lines—The Main 1 output delay line is approximately 10 feet in length using Times Microwave cable LMR-400-PVC CATV® (UL) plus 2 feet of semi-rigid coax and various N and GR connectors to select the final delay length. Coaxial cables were added to the Forward and Reflected path delays of the Main 2 path, and the phase shifters were adjusted to accommodate the Main 1 path fixed delay. After electrical alignment is set the Reflect path delay can be reduced to the minimum length possible. That same amount of delay removed from the Reflect path needs to be removed then from the Main path and the forward path to correctly match all signal paths. The delay lines for this particular assembly can be reduced considerably by more efficient and compact layout of the amplifiers and couplers.

Electrical Alignment

- Main amplifiers 1 and 2 should be independently aligned to match each other as best as possible in terms of gain, return lLoss, insertion phase and IMD versus input power and dc bias point.
- The VVA and Booster amplifier chain must be able to reproduce the input drive to the RFAL with minimum or no distortion. The Main 1 amplifier must be biased-on before Main 2 and before RF drive is turned on, otherwise excessive drive may be applied to the Main 2 amplifier due to excessive reflected power from Main 1.
- The Main 1 output delay and the reflect path electrical delay and VVA amplitude level are adjusted to obtain IMD cancellation at the output of the RFAL; there should be minimum effect to the fundamental power over the operational frequency range.
- The correcting input signal reflected from Main 1, which is then coupled through the reflected path, is attenuated, delayed and amplified by the Booster amplifiers. The signal from the Booster amplifiers must have the right amount of IMD signal level for cancellation of the Main 2 internally generated intermods and also an additional level sufficient to cancel the IMDs of the Main 1 at the output of the RFAL's coupler. (This assumes optimum signal phasing to cause cancellation of all IMDs.)
- The forward path VVA level is adjusted to drive the Main 2 amplifier to the same level as the

Main 1 amplifier. The forward path delay and VVA level are adjusted to obtain flat output power over the full operating frequency band. The forward delay should match the reflected path delay to achieve optimum cancellation of IMD and maximum combining of fundamental power.

- The DC Bias (I_q) point of both Main amplifier transistors are critical to achieve optimum cancellation. The bias point of both Main amplifiers can be adjusted slightly to find the best IMD cancellation versus input drive. The level of cancellation possible is interrelated to the level of intermod match performance of the two Main amplifiers over the operational drive levels and over the frequency band.

Further Improvements in IMD

The LDMOS transistors used for the Main 1 and Main 2 amplifiers for the presented RFAL assembly were not as well matched as expected. Ideally, it is desirable to have the output and reflected input intermods (IMD 3rd, IMD 5th, IMD 7th) to have a constant level difference over the input power range and operating frequency range.

(IM*x* out – IM*x* in) = (Constant dB value)

Ideally this constant dB value should be the same for *x* = 3rd, 5th, 7th, etc… intermods for both Main 1 and Main 2 amplifiers. A constant dB value allows a fixed amount of gain from the Booster amplifier chain to provide the correct level for perfect cancellation across the input drive and frequency ranges. (This assumes a perfect phase match.)

The constant dB value is not exactly the same for each transistor and may be different for specific quiescent values of the drain current (I_q). The ideal I_q value for each amplifier/transistor can be selected to provide the best performance trade-off over the input drive and over the operating frequency range. Normally the optimum I_q value for the Main amplifier's transistor used in the RFAL configuration would be lower than the "sweet-spot" bias point found for IM3 in most data sheets for the LDMOS transistor.

To increase the level of match between the main amplifiers, an approach similar to that used for the manufacturing of CATV push-pull hybrid amplifiers or push-pull power transistors in a single package could be used. For CATV amplifiers the transistor die is selected so that the set is picked from adjacent locations in the transistor wafer. Preferably, although more costly, the transistors can be manufactured as a MMIC set. This will increase the level of match and improve the level of IMD cancellation over a wider input drive level.

Thermal Issues

The RFAL allows operation of the transistors at higher RF power levels where the transistors are more efficient while providing acceptable cancellation of the unwanted distortion. Higher efficiency in amplifiers corresponds to lower dissipated power and results in smaller heat sink and cooling necessary for reliable operation. The RFAL uses two power transistors to achieve the desired output power level. Separation of these heat sources results in more effective cooling and longer operating life.

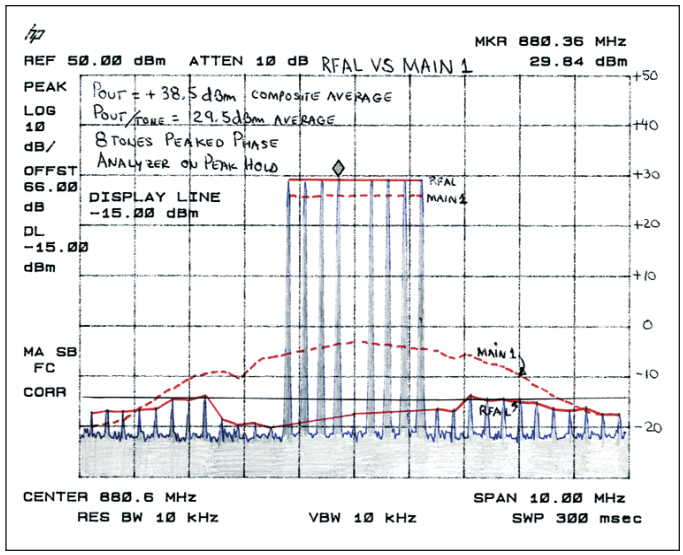

Figure 5 · RFAL vs. Main 1 amplifier (spectrum with 8 carriers peaked phase and peak hold).

Performance and Cost Issues

The RFAL uses smaller geometry type transistors to achieve the same level of operational power without heavy OPBO for a given level of IMD (OPBO = Operating Back-Off Point from 1 dB compression). Smaller geometry transistors are cheaper and easier to match over a wider operating bandwidth. Since only two transistor stages are used, the task of adjusting the delay lines and amplitude levels is easier than in multistage-type feedforward amplifiers. However, a high level of accuracy in amplitude and phase control is necessary to achieve >15 dB of cancellation, as is required for the feedforward amplifier configuration. The amplitude and level control can be more manageable if the transistors are carefully matched before constructing the Main amplifiers and by careful temperature compensation of the Booster amplifier chain.

Conclusion

The RFAL architecture provides a useful alternative for the design of low distortion power amplifiers. It provides:

- High level of IMD cancellation with simple circuit configuration.
- High operating efficiency (>20% overall efficiency is possible)

- Lower transistor power dissipation, which correlates to improved thermal design
- Achieves operational power with low distortion using economical transistors
- Potential for dense packaging using microcircuit hybrid assembly or MMIC.

Acknowledgments

Thanks to Edward Lau formerly from Agere Systems and now with Ciclon Semiconductor for his support. Also thanks for the trimmer capacitor samples provided by Tronser, Inc., and thanks to Soshin Electronics for their miniature LTCC couplers.

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